High Speed Counter
IC610MDL110

The High Speed Counter module (HSC) allows a Series One or Series One Plus PC to monitor and control a number of process variables (position, velocity, flow rate) that the CPU cannot control due to timing constraints. A logical relationship between the counters seven inputs, the preset, and current value determines the status of its own two external outputs as well as others through CPU user logic. Figure 6.41 illustrates this concept.

The module can be installed in any of the first 4 I/O slots adjacent to the CPU, and uses 8 I/O and 2 counter references to interface with user logic. Indicators on the front face of the module give output and count status.

General Specifications	
Up/Down Counter Inputs	Increment (Up) Count Decrement (Down) Count Reset/Marker Preset Value (0 - 9999) Current Value (0 - 9999)
Up/Down Counter Outputs	Two Discrete DC (5 - 24 V) Current Value (BCD)
Reaction Time	< 100 Microseconds Between Pulse Received and Transition of Output
Environmental	
Operating Temperature	0 to 60° C
Humidity, Non-Condensing	5 to 95 %
Power Consumption from Internal Supply	70 mA @ 9 V dc
Pulse Rate	Without Filter < 10 kHz With Filter < 500 Hz (Filter selection by three dip switches on module, see page 6-69)
Range	0 to 9999 Binary Coded Decimal(BCD)
Minimum Pulse Width	25 mS

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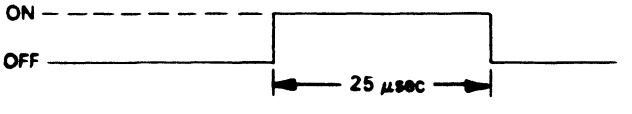

Module Location

The High Speed counter module (HSC) can be installed in any one of the four I/O slots adjacent to the CPU slot in the CPU chassis. In figure 6.42, these slots are shown (A, B, C and D) for a 5-slot rack. In a 10-slot rack, the HSC must also occupy 1 of the 4 slots adjacent to the CPU. Also shown in this figure are the I/O references used by the HSC to interface with user logic. Note how an HSC located in Slot A uses I/O references associated with both Slot A (0-3) and Slot A' (100-103).

Since each slot in a Series One or Series One Plus PC I/O system corresponds to a special group of eight I/O references, an HSC in Slot A eliminates Slot A' from the I/O system. Likewise an HSC located in Slot B eliminates Slot B' from the I/O system. In summary, an HSC physically occupies one I/O slot, but requires two slots worth of I/O references to interface with user logic (Refer to table 6.5).

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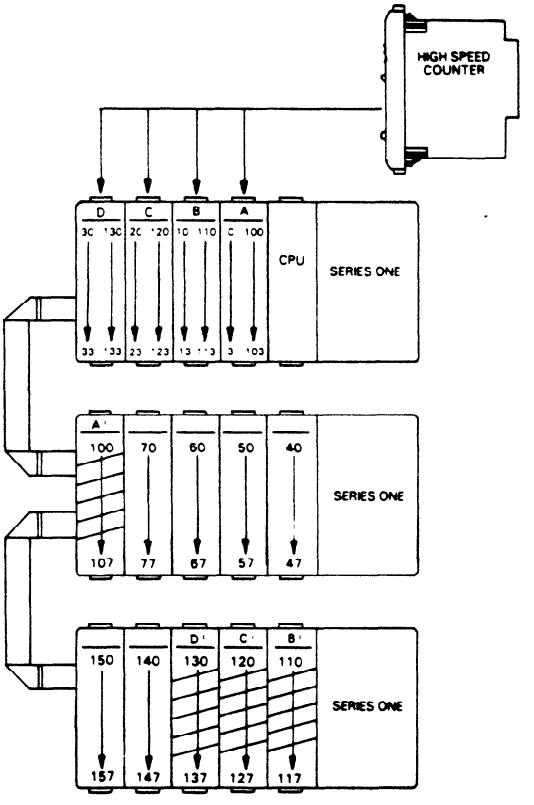

Figure 6-42. HSC Location in 5-Slot Rack

Table 6-5. Number of HSCs vs Discrete I/O Capacity

NUMBER OF HIGH SPEED COUNTER MODULES IN SYSTEM	REMAINING DISCRETE I/O CAPACITY	
	Series One	Series One Plus
0	112	168
1	96	152
2	80	136
3	64	120
4	48	104

Interface to Field Devices

A 32 PIN Connector (Refer to figure 6.43) on the faceplate of the HSC is the interface between the module and its associated field devices which include:

1. Counting mechanism which controls the Up/Down counter (typically a bi-directional incremental encoder).
2. Four digit binary coded decimal (BCD) display of counters current value.
3. Two 5 to -24 V dc loads under control of two counter outputs.

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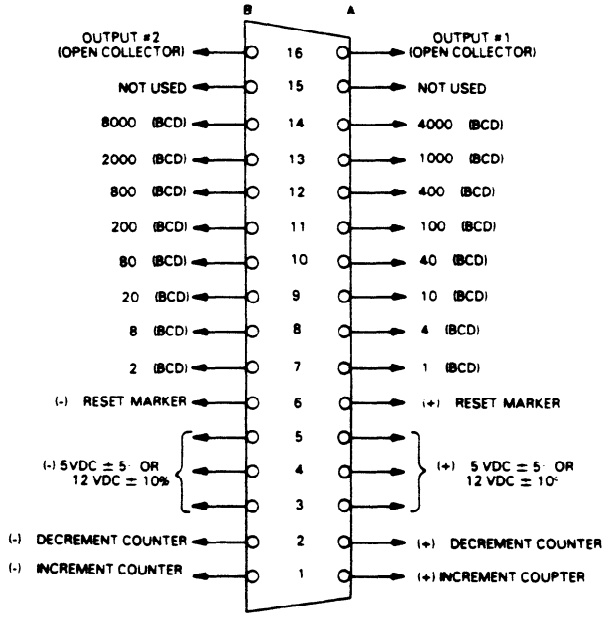

Figure 6-43. HSC Connector Pin Definition

In the interest of clarity the specifications for each field device are addressed separately.

Up/Down Counter Inputs

SPECIFICATIONS		
ITEM	UP/DOWN INPUT	RESET INPUT
Minimum Input Pulse Width	25 nSec	100 nSec
Supply Voltage	+12 V dc, 10%	+12 V dc, 10%
On Current	< 3 mA	10 to 15 mA
Off Current	10 to 15 mA	< 3 mA
On Voltage	< 3 V dc	> 7 V dc
Off Voltage	> 7 V dc	< 3 V dc

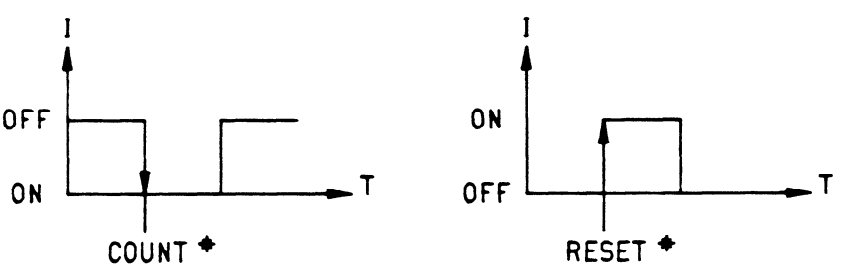

Figure 6-44. Signal Direction

The conditions necessary to increment/decrement, or reset the counter are described below. This is of particular interest when counting in one direction only.

DESIRED ACTION	CONDITION
Increment Current Count	Increment Input: (Disabled) -- (Enabled) Decrement Input: Disabled Reset Input: Disabled
Decrement Current Count	Decrement Input: (Disabled) -- (Enabled) Increment Input: Disabled Reset Input: Disabled
Reset Current Count	Reset Input: (Disabled) -- (Enabled) Increment Input: Disabled or Enabled Decrement Input: Disabled or Enabled
Increment Input:	Disabled, > 10 V dc Between Pins B1 and A1 Enabled, < 2 V dc Between Pins B1 and A1
Decrement Input:	Disabled, > 10 V dc Between Pins B2 and A2 Enabled, < 2 V dc Between Pins B2 and A2
Reset Input:	Disabled, < 2 V dc Between Pins B6 and A6 Enabled, > 10 V dc Between Pins B6 and A6

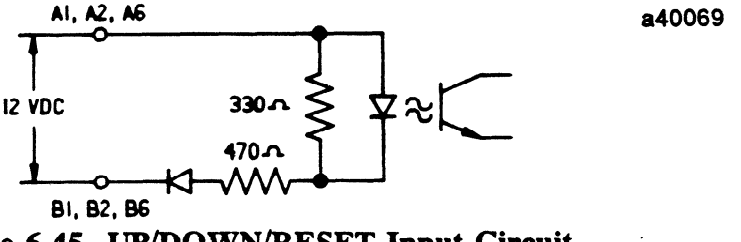

Figure 6-45. UP/DOWN/RESET Input Circuit

Encoder Interface 1

Typically an incremental encoder controls the counter through the Up/Down, and Reset Inputs. To comply with HSC circuitry, the encoder should represent clockwise and counterclockwise movement of its shaft with two separate pulse trains that increment and decrement the counter. Figures 6.46, 6.47, and 6.48 illustrate sample connections.

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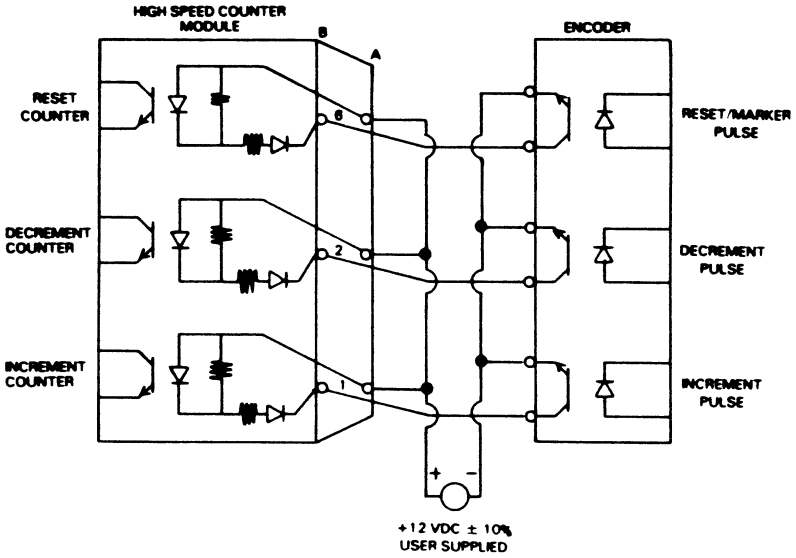

Figure 6-46. Encoder with RESET/MARKER Option Resetting Counter Once per Revolution of Encoder Shaft

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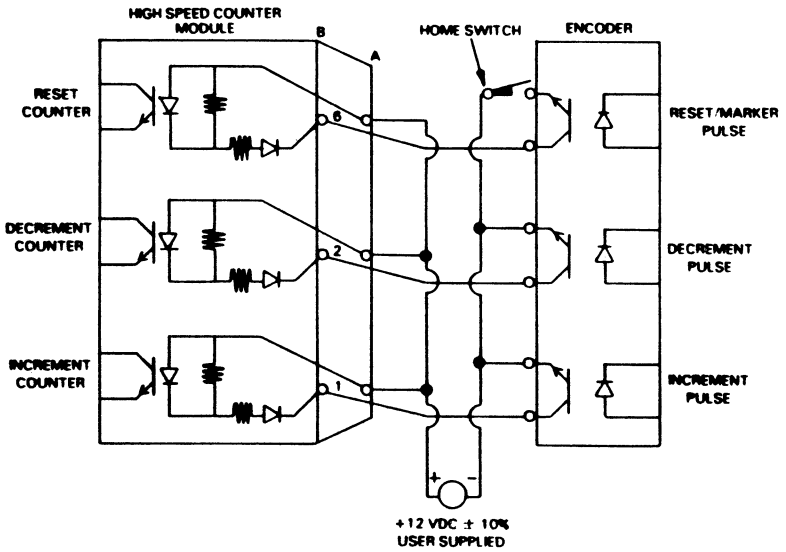

Figure 6-47. Encoder with RESET Option in Series with Home Limit Switch Such That Counter is Reset When Both Home Limit Switch and RESET/MARKER Pulse are Enabled

pc-s1-84-0007

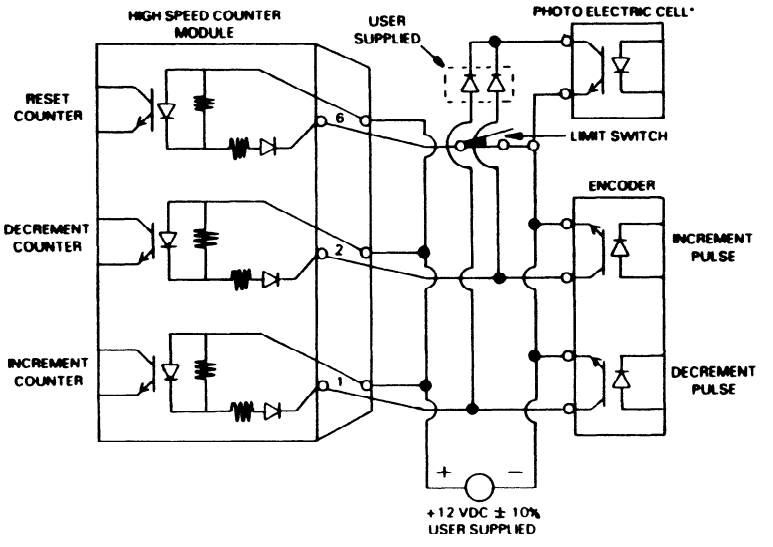

Figure 6-48. Encoder With Limit Switch Resetting Counter and Photoelectric Cell Inhibiting the Counter Operation

Binary Coded Decimal (BCD) Output

To view the counter current value, a four digit BCD (sink/source) output is provided.

SPECIFICATIONS		
ITEM	**RATING**	
OUTPUT POLARITY	1: Optoisolator OFF 0: Optoisolator ON See Sample Circuit Below	
SOURCE MODE Supply Voltage Allowable Ripple Current Consumption Output Voltage	 5 V dc 5% < 1% < 10 mA 3.5 V dc at 0.1 mA	 12 V dc + 10% < 3% < 25 mA 6 V dc at 0.4 mA
SINK MODE Output Voltage	 0.4 V dc @ 2 mA 0.1 V dc @ 3 mA	

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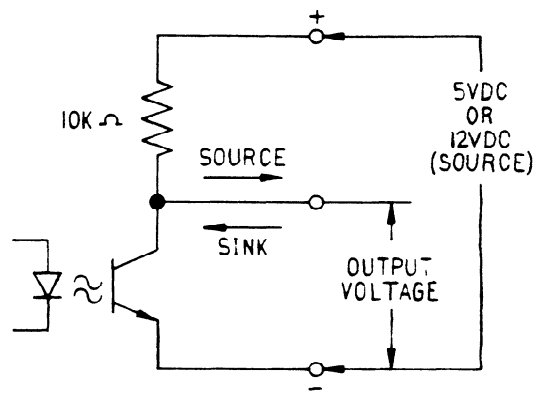

Figure 6-49. Sample BCD Output Circuit

Figure 6.50 illustrates the connections necessary to use an external BCD Display. For a source type output the 5 V or 12 V supply is required.

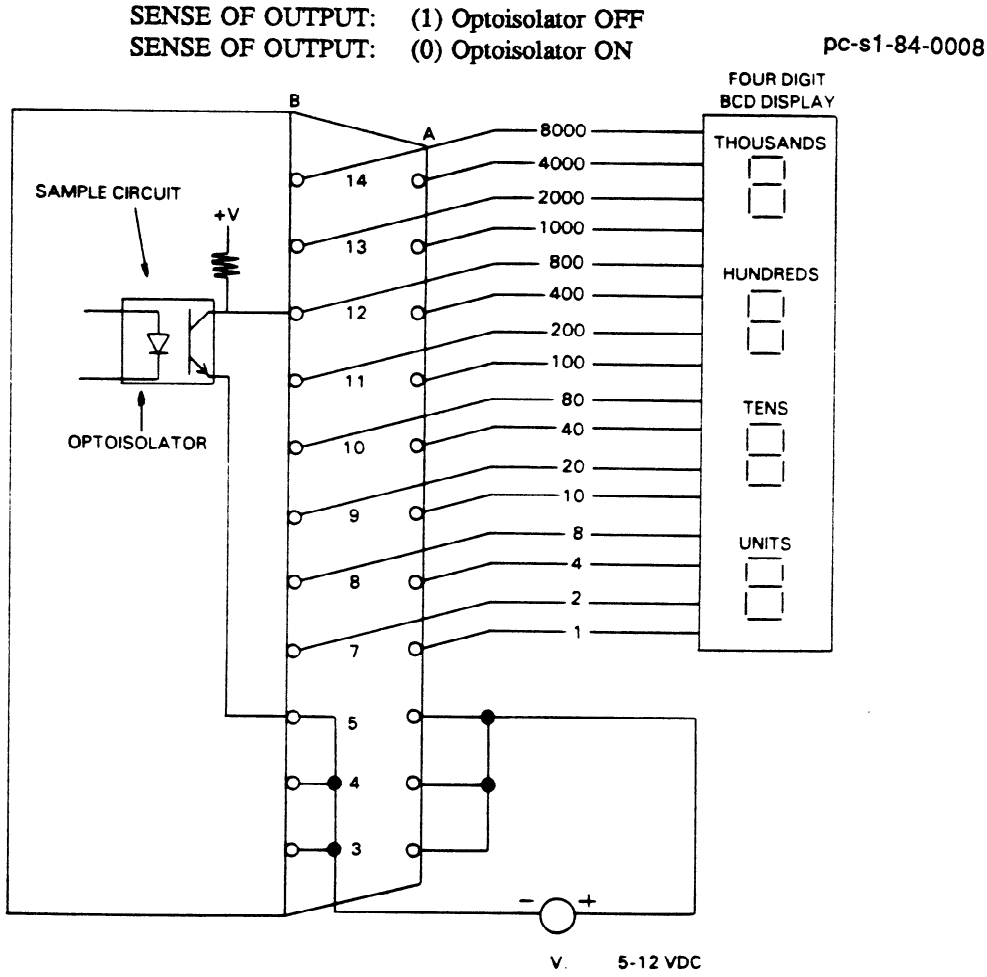

Figure 6-50. BCD Output Wiring Diagram

Counter Output

The HSC has two discrete outputs that can be controlled from ladder logic or by the relationship (>=<) between the present and current value of the counter.

SPECIFICATIONS	
ITEM	**RATING**
Type	NPN Transistor, open collector, sinking
Voltage Range	5 to 24 V dc
Peak Voltage	< 45 V dc
Current Range	> 0.3 A

A typical wiring schematic to field devices and a sample circuit are shown in figure 6.51.

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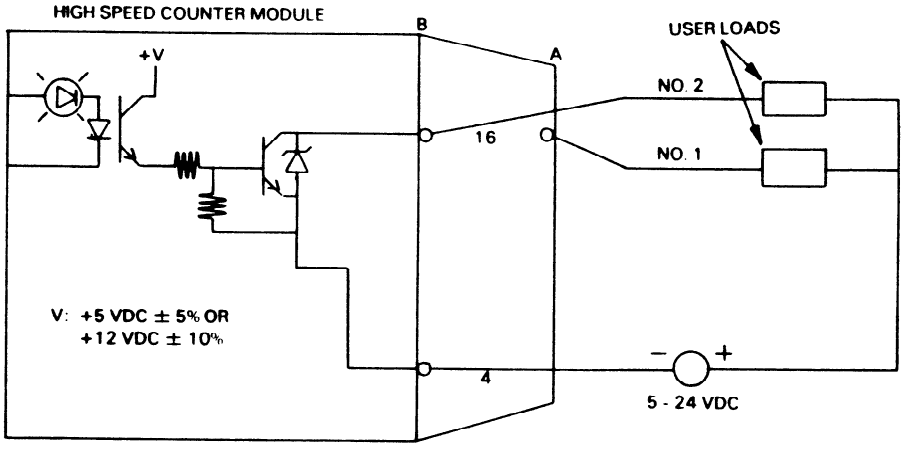
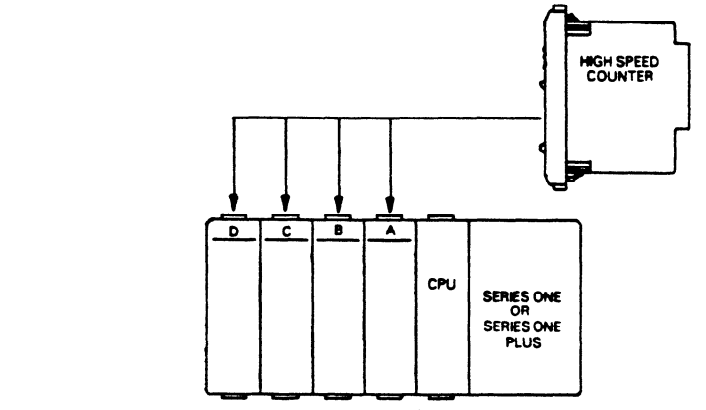


Figure 6-51. User Load Wiring Diagram

Interface to User Logic

Eight I/O and two counter functions interface the HSC to user logic. The specific references associated with these functions depend upon the location of the module in the CPU rack. Figure 6.52 illustrates how these references correspond to the modules location.

pc-s1-84-0011



COUNTER FUNCTION	COUNTER REFERENCES			
SET CURRENT VALUE	106	104	102	100
PRESET VALUE	107	105	103	101
INPUT FUNCTION	**INPUT REFERENCES**			
> PRESET VALUE	30	20	10	00
= PRESET VALUE	31	21	11	01
< PRESET VALUE	32	22	12	02
CARRY/BORROW	33	23	13	03
OUTPUT FUNCTION	**OUTPUT REFERENCES**			
OUTPUT NO. 1 STATE	130	120	110	100
OUTPUT NO. 1 MODE SELECT	131	121	111	101
OUTPUT NO. 2 STATE	132	122	112	102
OUTPUT NO. 2 MODE SELECT	133	123	113	103

Figure 6-52. I/O and Counter Function Reference Chart

Interface Function Definition

Shown below is the definition and user logic symbol for each interface function.

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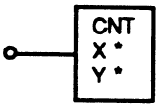
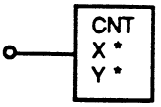
COUNTER FUNCTIONS	USER LOGIC SYMBOL	DEFINITION
SET CURRENT VALUE	 X: 100, 102, 104, 106 Y: 0 - 9999	WHEN COUNTER X IS ENABLED, CURRENT COUNT IS SET TO A VALUE OF Y
PRESET VALUE	 X: 101, 103, 105, 107 Y: 0 - 9999	WHEN COUNTER X IS ENABLED, PRESET VALUE OF COUNTER IS SET TO Y

* X = Counter Reference
* Y = Valid Range

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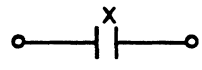
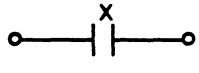
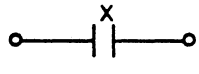
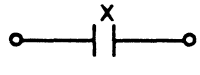
INPUT FUNCTIONS	USER LOGIC SYMBOL	DEFINITION
> PRESET VALUE* *	 X: 00, 10, 20, 30	ENABLED WHEN CURRENT VALUE OF COUNTER IS GREATER THAN ITS PRESET VALUE
= PRESET VALUE* *	 X: 01, 11, 21, 31	ENABLED WHEN CURRENT VALUE OF COUNTER IS EQUAL TO ITS PRESET VALUE
< PRESET VALUE* *	 X: 02, 12, 22, 32	ENABLED WHEN CURRENT VALUE OF COUNTER IS LESS THAN ITS PRESET VALUE
CARRY / BORROW	 X: 03, 13, 23, 33	*

* Enabled when current value of the counter undergoes one of the six sequences described below :

1. 0001 - 0000 - 9999 (Decrement Rollover)
2. 9999 - 0000 - 0001 (Increment Rollover)
3. 0001 - 0000 - 0001
4. 9998 - 9999 - 9998
5. (Increment Current Count) - (Externally Reset Counter) - (Decrement Current Count)
6. (Decrement Current Count) - (Externally Reset Counter) - (Increment or Decrement Current Count)

* * The status of these input functions is given to the CPU once per scan. Therefore, if a particular condition is true for less than the scan time of the user logic, its associated Input function would not be enabled in the user program.

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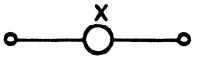
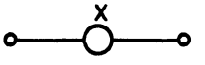
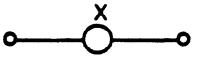
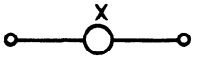
OUTPUT FUNCTIONS	USER LOGIC SYMBOL	DEFINITION *
OUTPUT NO. 1 MODE SELECT	 X: 101, 111, 121, 131	• IF DISABLED OUTPUT NO. 1 IS IN MANUAL MODE • IF ENABLED OUTPUT NO. 1 IS IN COUNTER MODE
OUTPUT NO. 1 STATE	 X: 100, 110, 120, 130	• IN MANUAL MODE OPERATES OUTPUT NO. 1 AS NORMAL OUTPUT • IN COUNTER MODE DETERMINES IF OUTPUT NO. 1 IS ENABLED BEFORE OR AFTER PRESET IS REACHED
OUTPUT NO. 2 MODE SELECT	 X: 103, 113, 123, 133	• IF DISABLED OUTPUT NO. 2 IS IN MANUAL MODE • IF ENABLED OUTPUT NO. 2 IS IN COUNTER MODE.
OUTPUT NO. 2 STATE	 X: 102, 112, 122, 132	• IN MANUAL MODE OPERATES OUTPUT NO. 2 AS NORMAL OUTPUT • IN COUNTER MODE DETERMINES IF OUTPUT NO. 2 IS ENABLED BEFORE OR AFTER PRESET IS REACHED

* For further description on the operation of outputs, refer to Output Logic Section.

Ouptut Logic

Each of the two HSC outputs operate in either the manual or counter mode. The operating mode of each output is determined by the state of its mode select function (refer to output function section). The logic of each mode will be covered separately.

If Mode Select Function Disabled (0): Manual Mode, Enabled (1): Counter Mode.

Manual Mode

The state of an output in the manual mode corresponds to the status of its associated Output State Function as shown below in the manual mode output truth table.

Table 6-6. Manual Mode Output Logic Truth Table

OUTPUT MODE SELECT	OUTPUT STATE	OUTPUT
0	0	0
0	1	1

Counter Mode

In the counter mode of operation outputs can react immediately when the current count reaches specific preset values. In this mode each output is controlled by a combination of three factors.

1. Initial relationship between preset and current count.
2. Real time relationship between preset and current count.
3. Status of Output State function.

When the HSC receives a preset value from user logic (via preset counter function), it is initially compared to the current value of the counter. If the preset is greater than the current count in this initial comparison the real time comparison*[2]between the preset and current count is "true" when the current count is greater than or equal to the preset. In other words when the current count reaches the preset moving in the POSITIVE direction the real time comparison becomes "true". This concept is shown below in table 6.7.

Table 6-7. Real Time Comparison Table for Preset Initially > Current Count

	CURRENT COUNT < PRESET	CURRENT COUNT ≥ PRESET
REAL TIME COMPARISON STATUS	FALSE	TRUE

*Real Time Compariston = continuous comparison between preset value and current value of counter.

Conversely, if the preset is initially less than the current count, the real time comparison is "true" when the current count is less than or equal to the preset. In other words, when the current count reaches the preset moving in the negative direction the real time comparison becomes "true". This concept is shown below in table 6.8.

Table 6-8. Real Time Comparison Table for Preset Initially < Current Count

	CURRENT COUNT > PRESET	CURRENT COUNT < PRESET
REAL TIME COMPARISON STATUS	FALSE	TRUE

Once the status of the real time comparison between the preset and current count has been determined, the status of the output is easily obtained. If the outputs associated output state function is disabled its status corresponds directly to the real time comparison status. If the output state function is enabled the output's status is the inverse of the real time comparison status. This concept is shown in table 6.9.

Table 6-9. Output State vs Real Time Comparison Status in Counter Mode

OUTPUT STATE FUNCTION	REAL TIME COMPARISON IS FALSE	REAL TIME COMPARISON IS TRUE
DISABLED ENABLED	0 1	1 0
1: OUTPUT ENABLED **0: OUTPUT DISABLED**		

Table 6.10 summarizes the logic associated with an output in the counter mode of operation.

Table 6-10. Output Logic in Counter Mode

INITIALLY PRESET > CURRENT COUNT		
OUTPUT STATE FUNCTION	CURRENT COUNT < PRESET	CURRENT COUNT ≥ PRESET
0	0	1
1	1	0
INITIALLY PRESET < CURRENT COUNT		
OUTPUT STATE FUNCTION	CURRENT COUNT > PRESET	CURRENT COUNT < PRESET
0	0	1
1	1	0

Filter Selection

In some electrical noisy environments it may be necessary to filter out noise through filters available on the module. The HSC provides this capability on the incremental count, decremental count, and reset/marker inputs. The location of these switches on the module is shown in figure 6.53.

Sense of switch: OPEN - Filter Disabled (< 10 Khz)
CLOSED - Filter Enabled (< 500 Hz)

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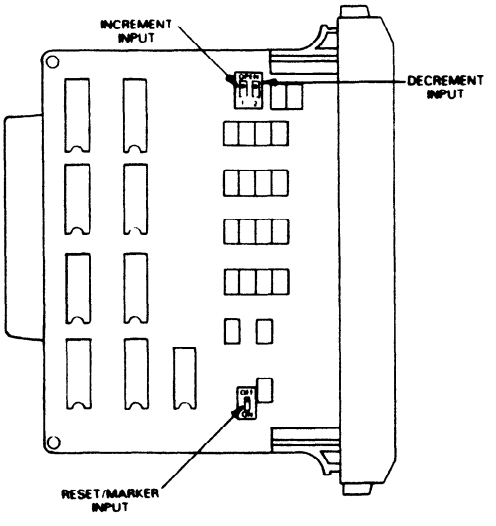

Figure 6-53. Filter Selection with Dip Switch